Coryell & Wiprud

EV-4114

Quad Transmitter Board

Data Sheet

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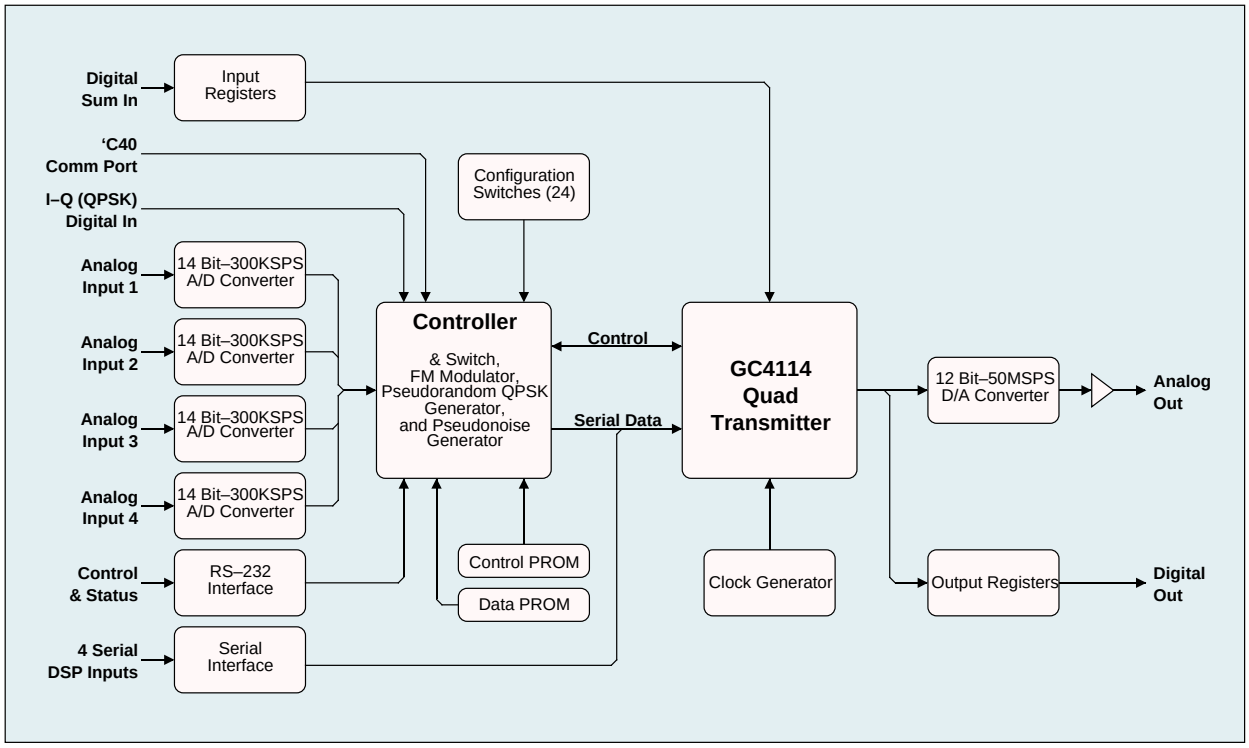
1.0 Summary of Features

The Coryell & Wiprud EV–4114 is designed to accelerate the evaluation of Graychip's GC4114 Quad Transmitter Chip. The GC4114 can be exercised using a simple test setup consisting of the EV–4114, a spectrum analyzer, and a power supply. One of 32 sets of GC4114 register configurations and one of several signal types can be selected by dip-switches.

Further testing may be accomplished using the high speed RS–232 port to program the GC4114 and a variety of analog and digital signal input ports. There are 4 analog inputs driving 14 bit, 300 KSPS, analog to digital converters. The EV–4114 can be driven digitally by almost any DSP chip using either serial ports, or a TMS320C40 style comm port. A symbol-serial I–Q Interface is provided for QPSK generation and a digital FM modulator can be driven by one of the A/Ds. Pseudonoise, Pseudorandom QPSK, and CW signals can be generated internally. Output signals are monitored using either a 12 bit, 50 MSPS, digital to analog converter, or a 16 bit digital output.

Multiple EV–4114s can be daisy-chained together using the 16 bit digital input and 16 bit digital output to generate 8, 12, or more channels. Clocks are generated from the digital input, and external source, or from an on-board 50 MHz oscillator.



1.1 Summary of Operation

The EV-4114 is designed for stand-alone operation or under manual or computer control. By changing dip switch settings, up to 32 different configurations can be loaded with the push of a button. Additional variations on these 32 basic configurations are possible by selecting various input sources and modulations.

Additionally, there is complete flexibility in configuring the Graychip GC4114 after the EV-4114 has been configured. An external computer can read or write any register within the GC4114 via the RS-232 connector.

1.2 Static Sensitivity Warning

The EV-4114 contains static sensitive circuitry. Do not remove the EV-4114 from its protective shipping wrapper unless in a static-controlled area. Proper static control procedures must be followed to prevent damage to the board, especially during connection of external cabling.

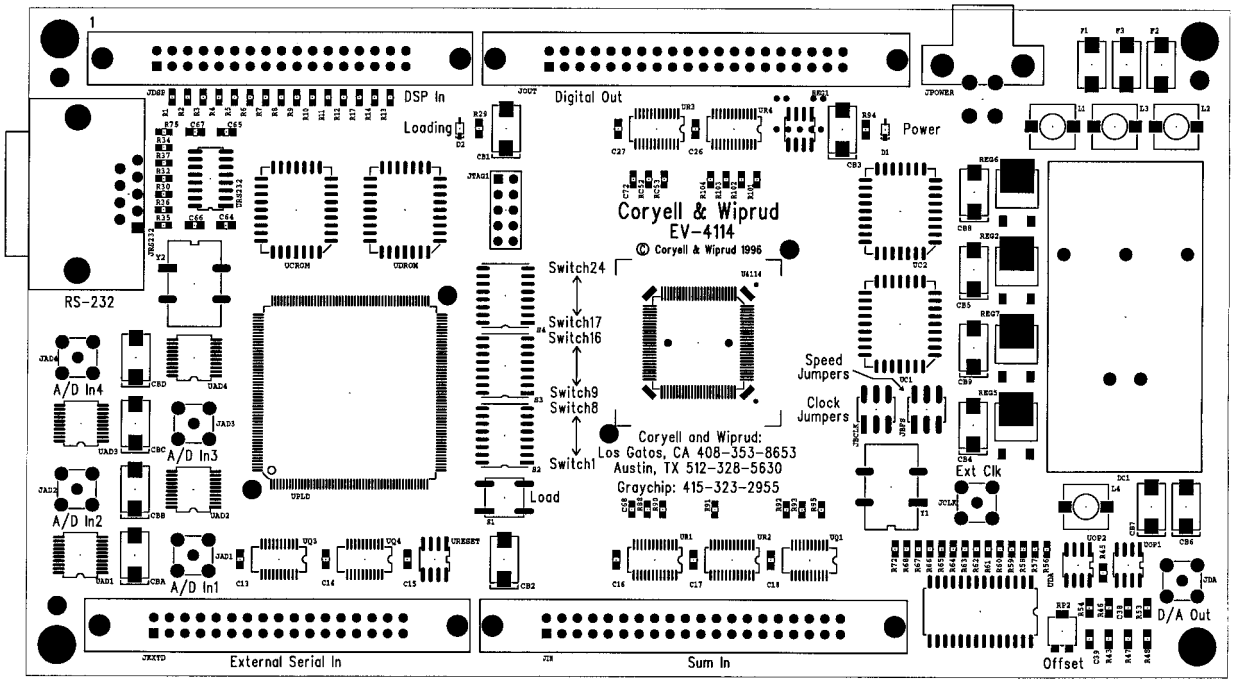
2.0 Preparing the board for operation

As shipped, the EV-4114 board is almost ready to go. To use the board, connect a 5 volt power supply to the connector labeled JPOWER, connect analog inputs to JAD1 through JAD4 (as desired), and monitor the output via the JDA connector.

There are a number of user-configurable settings on the EV-4114, some of which are interlinked. Please take a few moments to familiarize yourself with the switch and jumper settings which follow.

2.1 Switch & Jumper Settings

The following section describes the function of each switch on the board. There is a single pushbutton switch (S1), and there are three banks of 8-bit dip switches (labeled S2, S3 and S4 on the board), totaling 25 configuration switches. Each dip switch has been assigned a number starting from Switch1. These numbers are also on the board silkscreen, and are referred to in the following tables by the abbreviation SW. The default settings have been highlighted in **bold**. In addition, there are two 2x3 pin jumper blocks used for clock configuration.



2.2 Load Switch

This pushbutton switch causes the board to be reset. Upon reset, the board will configure the GC4114 based upon the dip switch settings (SW8..SW4). Following configuration, the board is active and will respond to RS-232 commands.

2.3 Configurations Switches

There are 3 sets of 8 configurations switches labeled Switch1 through Switch24 on the board. This section describes the operation of each of these switches. The switches are abbreviated SWxx, where xx is the switch number. A range of switches is abbreviated SWxx..yy, where xx is the highest numbered switch and yy is the lowest numbered switch.

2.3.1 RS-232 Interface (SW2..1)

Switch	Setting	Meaning
SW2..SW1	Off,Off	9600 Baud RS-232 interface
SW2..SW1	**Off,On**	19200 Baud RS-232 interface
SW2..SW1	On, Off	57600 Baud RS-232 interface
SW2..SW1	On, On	115200 Baud RS-232 interface

The RS-232C interface conforms with the full +/- 15V signaling levels required by the specification. However, the handshake lines (RTS, CTS, DTR, etc.) are not used. The board drives transmitted serial data on to pin 2 of JRS232 (a DB9 female type connector) and expects to receive incoming serial data on pin 3. These signals are received relative to the board ground on pin 5.

The format of the serial word for both transmission and reception is 1 start bit, 8 data bits, 1 stop bit, and no parity.

There are two commands understood by the RS-232 interface command interpreter, a read and a write. These commands are designed to control the GC4114 with a minimum of overhead, yet allow manual operator control.

The read command is “Raa<CR>” where R is the literal ASCII character 82, aa is an ASCII-HEX address ranging from 00 to 3F, and <CR> represents a carriage return (ASCII character 13). The response to a read command is “Raa<CR>dd<CR>” where dd is an ASCII-HEX representation of the data found at the given address.

The write command is “Waadd<CR>” where W is the literal ASCII character 87, aa is an ASCII-HEX address ranging from 00 to 3F, and <CR> represents a carriage return (ASCII character 13). The response to a write command is identical, namely “Waadd<CR>”.

If an illegal character is detected during command entry, the command is aborted and the character “?” (ASCII character 63) is returned.

2.3.2 Reserved (SW3)

Switch	Setting	Meaning
SW3	**Off**	reserved

2.3.3 Starting Configuration (SW8..4)

The EV-4114 loads one of 32 register configurations into the GC4114 chip at power up or whenever the *LOAD* button is pressed. The *LOAD* LED will be illuminated whenever GC4114 registers are being set. These register configurations may serve as reference configurations for development of new configurations. To load a particular configuration, set the configuration number using Switches 4 through 8, and press the *LOAD* button.

In order to make developing custom register settings easier, register settings are echoed to the RS-232 port during loading so they can be captured by a terminal emulation program. The user may then modify the settings as desired and download them back to the the EV-4114

Switch	Setting	Meaning
SW8..SW4	Decimal	Boot action setting. (one of 32)
"00000"	**0**	Channel A Only; 10 MHz; DC Input
"00001"	1	Channel C Only; 11 MHz; DC Input
"00010"	2	Channel C Only; 12 MHz; DC Input
"00011"	3	Channel D Only; 13 MHz; DC Input
"00100"	4	Channels A and B Only; 10 and 11 MHz; DC Input
"00101"	5	Channels C and D Only; 12 and 13 MHz; DC Input
"00110"	6	All 4 Channels; 10, 11, 12, and 13 MHz; DC Inputs
"00111"	7	Same as 12 Except External Filter
"01000"	8	Same as 0 Except 25 KSPS Real Input
"01001"	9	Same as 1 Except 25 KSPS Real Input
"01010"	10	Same as 2 Except 25 KSPS Real Input
"01011"	11	Same as 3 Except 25 KSPS Real Input
"01100"	12	Same as 4 Except 25 KSPS Real Inputs
"01101"	13	Same as 5 Except 25 KSPS Real Inputs
"01110"	14	Same as 6 Except 25 KSPS Real Inputs
"01111"	15	Same as 20 Except External Filter
"10000"	16	Same as 0 Except 25 KSPS Complex Input
"10001"	17	Same as 1 Except 25 KSPS Complex Input
"10010"	18	Same as 2 Except 25 KSPS Complex Input
"10011"	19	Same as 3 Except 25 KSPS Complex Input
"10100"	20	Same as 4 Except 25 KSPS Complex Inputs
"10101"	21	Same as 5 Except 25 KSPS Complex Inputs
"10110"	22	Same as 6 Except 25 KSPS Complex Inputs
"10111"	23	Same as 28 Except External Filter
"11000"	24	Same as 0 Except 250 KSPS Complex Input
"11001"	25	Same as 1 Except 250 KSPS Complex Input
"11010"	26	Same as 2 Except 250 KSPS Complex Input
"11011"	27	Same as 3 Except 250 KSPS Complex Input
"11100"	28	Same as 4 Except 250 KSPS Complex Inputs
"11101"	29	Same as 5 Except 250 KSPS Complex Inputs
"11110"	30	Same as 6 Except 250 KSPS Complex Inputs
"11111"	31	No Signal; All Channels Off

The configurations described by the above table are useful for stand-alone demonstrations of the GC4114 capabilities. When other configurations are required, they can be invoked via the RS-232 interface.

2.3.4 External Serial Data Source (SW9)

Switch	Setting	Meaning
SW9	Off	Source of SFS/SCK/SIN signals is JExtD connector
	On	Board generates SFS/SCK/SIN signals

If external serial signal sources are desired, the JExtD connector is used to accept them. A copy of the REQ signal, as well as system sync, bit rate clock, and bit sync signals are sent to the JExtD connector to coordinate the external system.

2.3.5 Port A Input Selection (SW10)

Switch	Setting	Meaning
SW10	**Off**	Port A data is from A/D (JAD1)
	On	Port A data is FM or PM of data from A/D (JAD1)

When this switch is on, the FM vs PM selection is controlled by switch SW15. The index of modulation is controlled by switches SW24..SW21.

2.3.6 Port B Input Selection (SW11)

Switch	Setting	Meaning
SW11	**Off**	Port B data is from A/D (JAD2)
	On	Port B data is from Comm Port (JDSP)

The data format for words received from the Comm port is 16-bit pairs of words fitted into each 32-bit Comm port transfer. For example, if the data word 0xAABBCCDD were loaded into a 'C40 Comm port for output, the GC4114 would see two 16-bit transfers of the values 0xCCDD followed by 0xAABB. Since the GC4114 expects data to arrive In-phase followed by Quadrature, the MSBs of the 32-bit word must hold the Quadrature value.

2.3.7 Port C Input Selection (SW12)

Switch	Setting	Meaning
SW12	**Off**	Port C data is from A/D (JAD3)
	On	Port C data is bit stream data from JDSP

The In-phase and Quadrature data from the bit stream (JDSP or pseudorandom depending on SW14 setting) are converted to full-scale, signed, 16-bit data and sent to the GC4114. A “0” data bit maps to 0x8000, while a “1” input maps to 0x7FFF.

2.3.8 Port D Input Selection (SW13)

Switch	Setting	Meaning
SW13	**Off**	Port D data is from A/D (JAD4)
	On	Port D data is pseudorandom

The pseudo-random data is generated by a 22-tap linear feedback shift register.

2.3.9 Bit Stream Source Selection (SW14)

Switch	Setting	Meaning
SW14	**Off**	Bit streamis from IData/QData on JDSP connector
	On	Bit stream is pseudorandom

The bit stream is only used when SW12 is on.

2.3.10 Modulation Type (SW15)

Switch	Setting	Meaning
SW15	**Off**	Frequency modulate JAD1 input
	On	Phase modulate JAD1 input

The modulated output is only used when SW10 is On. The index of modulation is determined by SW24..SW21.

2.3.11 Reserved (SW16)

Switch	Setting	Meaning
SW16	**Off**	reserved

Board Configuration Dipswitch (S4)

2.3.12 PLL Frequency Range (SW17)

Switch	Setting	Meaning
SW17	**Off**	GC4114 Operates in 25-50 MHz range
	On	GC4114 Operates in 15-30 MHz range

Set this switch to match the frequency of operation for the board. Normal operation from the on-board crystal oscillator will require this switch to be off. When external clocks are in use, (See JBCLK jumper settings) this switch may have to be changed.

2.3.13 PLL Disable (SW18)

Switch	Setting	Meaning
SW18	**Off**	PLL enabled for normal operation
	On	PLL disabled

The on-board PLL circuit locks to the board clock reference (See JBCLK jumper settings) and provides zero-skew clocks to all circuits on the board. Disabling the PLL makes it operate like a buffer, introducing delay between the reference clock and those on the board.

2.3.14 Reserved (SW19)

Switch	Setting	Meaning
SW19	**Off**	Reserved

2.3.15 Digital Output Enable (SW20)

Switch	Setting	Meaning
SW20	**Off**	Digital Outputs (JOUT) enabled
	On	Digital Outputs disabled

When they are not in use, disabling the digital outputs may reduce noise in the A/D and D/A circuitry.

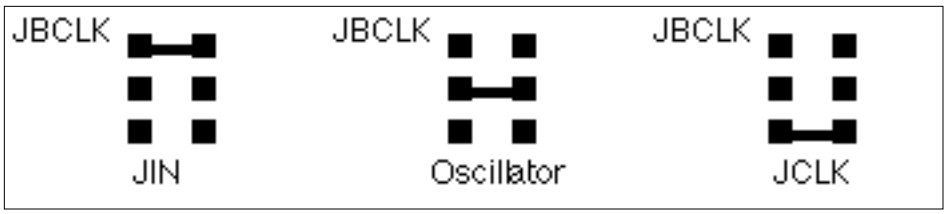
2.3.16 Modulation Index Selection (SW24..21)

Switch	Setting	Meaning
SW24..SW21	Binary	Selects index of modulation
	0	Default
	1	TBD
	2	TBD
	3	TBD
	4	TBD
	5	TBD
	6	TBD
	7	TBD
	8	TBD
	9	TBD
	10	TBD
	11	TBD
	12	TBD
	13	TBD
	14	TBD
	15	TBD

This modulation is applied to the data from A/D 1 (JAD1). The modulation represents FM or PM depending on SW15. The resulting modulated stream is only used if SW10 is On.

2.4 Clock Source Selection

The board obtains a clock from an on-board crystal oscillator, the cascade data input (JIN), or from an external source (JCLK). The selection is done via a jumper block (JBCLK) as follows:



2.5 External Clock Rate Doubler

When the clock source jumper (JBCLK) is configured to accept a clock from the JCLK connector, the board is capable of doubling the external clock rate before using it. This is accomplished by setting the jumper block JBFS as follows:

Proper operation from either the on-board oscillator or the cascade clock input requires that JBFS be set in the normal mode.

3.0 Input Requirements

3.1 Analog Inputs (JAD1-4)

Input range: +/- 5 Volts

Input impedance: 50 Ω

Connector type: SMA

3.2 Communications Port (JDSP)

Input type: TTL, 33Ω series termination

Timing requirements: As specified by Texas Instruments for the TMS320C4x processor series.

Connector type: 34-pin IDC

Pinout: see below.

3.3 Bit Stream Input (JDSP)

Input type: TTL, 33Ω series termination

Timing Requirements: 15ns setup/ 15ns hold relative to IQClock

Connector type: 34-pin IDC

Pinout:

Pin	Type	Name	Function
1	N/C		
3	I	D0	Comm Data LSB
5	I	D1	Comm Data
7	I	D2	Comm Data
9	I	D3	Comm Data
11	I	D4	Comm Data
13	I	D5	Comm Data
15	I	D6	Comm Data
17	I	D7	Comm data MSB
19	I	/CREQ	Comm port mastership desired
21	O	/CACK	Comm port granted
23	I	/CSTRB	Comm data valid
25	O	/CRDY	Comm data accepted
27	O	IQCLK	Bit stream clock (rising edge samples)
29	I	IDATA	In-phase bit stream data
31	I	QDATA	Quadrature bit stream data
33	N/C		
Even	Pwr	Ground	All even pins are ground

3.4 Cascade Input (JIN)

Input type: TTL, unterminated

Input format: 16-bit Two's Complement with active-low sync

Timing requirements: 5ns setup/ 2ns hold relative to clock.

Connector type: 40-pin IDC

Pinout:

Pin	Type	Name	Function
1	N/C		
3	I	D15	Data MSB (Two's complement sign)
5	I	D14	Data
7	I	D13	Data
9	I	D12	Data
11	I	D11	Data
13	I	D10	Data
15	I	D9	Data
17	I	D8	Data
19	I	D7	Data
21	I	D6	Data
23	I	D5	Data
25	I	D4	Data
27	I	D3	Data
29	I	D2	Data
31	I	D1	Data
33	I	D0	Data LSB
35	I	/SI	system sync
37	N/C		
39	I	Clkin	Input clock
Even	Pwr	Ground	All even pins are ground

3.5 External Direct Control (JEXTD)

Input type: TTL, unterminated

Timing requirements: See GC4114 datasheet.

Connector type: 34-pin IDC

Pinout:

Pin	Type	Name	Function
1	N/C		
3	O	ExtREQ	Buffered copy of REQ pin
5	O	/ExtSI	System sync pulse
7	O	ExtSClk	Bit rate clock for serial data
9	O	/ExtSFS	Serial Frame Sync pulse
11	I	SIn-A	Serial input, port A
13	I	SCk-A	Serial input clock, port A
15	I	SFS-A	Serial input frame strobe, port A
17	I	SIn-B	Serial input, port B
19	I	SCk-B	Serial input clock, port B
21	I	SFS-B	Serial input frame strobe, port B
23	I	SIn-C	Serial input, port C
25	I	SCk-C	Serial input clock, port C
27	I	SFS-C	Serial input frame strobe, port C
29	I	SIn-D	Serial input, port D
31	I	SCk-D	Serial input clock, port D
33	I	SFS-D	Serial input frame strobe, port D
Even	Pwr	Ground	All even pins are ground

3.6 External Commands RS-232 (JRS232)

Input/Output type: RS-232C, +/- 15V

Connector type: DB9 Female

Pinout:

Pin	Type	Name	Function
1	N/C		
2	O	TxD	Transmitted data
3	I	RxD	Received data
4	N/C		
5	Pwr	Ground	Ground reference
6	N/C		
7	N/C		
8	N/C		
9	N/C		

3.7 Power Input (JPOWER)

Input requirement: +5 Volts +/- 5% only, TBD amperes.

Connector type: 4 Wire Power Socket

Pinout:

Pin	Type	Name	Function
1	Pwr	+5V	Board main power source
2	N/C		
3	Pwr	Ground	Board main power return
4	N/C		

4.0 Outputs

4.1 Cascade Output (JOUT)

Output format: 16-bit Two's Complement with active-low sync

Timing performance: 7ns clock to output.

Connector type: 40-pin IDC

Pinout:

Pin	Type	Name	Function
1	N/C		
3	O	D15	Data MSB (Two's complement sign)
5	O	D14	Data
7	O	D13	Data
9	O	D12	Data
11	O	D11	Data
13	O	D10	Data
15	O	D9	Data
17	O	D8	Data
19	O	D7	Data
21	O	D6	Data
23	O	D5	Data
25	O	D4	Data
27	O	D3	Data
29	O	D2	Data
31	O	D1	Data
33	O	D0	Data LSB
35	O	/SI	system sync
37	N/C		
39	O	Clkout	Output clock
Even	Pwr	Ground	All even pins are ground

4.2 Analog Output (JDA)

Output voltage range: +/- 1V

Output impedance: 50 Ω

Connector type: SMA

4.3 Power LED (D1)

Illuminated while +5V supply is present.

4.4 Loading LED (D2)

Illuminated while Graychip GC4114 is being configured from ROM. After this light goes out, RS-232 commands will be accepted. While any command from the RS-232 interface is in progress, this LED will be illuminated.

Appendices

A1 ROM Formats

UCROM - ASCII commands identical to RS232 format. 32 possible different programs, each starting at a unique address. Each program must be zero terminated.

UDROM - lookup table for FM/PM. The lower address is the 12-bit 2's complement data (x), while the data is sin(x). Switches 24-21 control the upper address bits, determining which section of this ROM will be used.

A2 RS-232 Command Format

RS-232 command formats There are 6 bits of address used by the GC4114, so valid addresses are from 0x00 to 0x3F.

Read

```
Command : R<hex digit><hex digit><cr>

Response: R<hex digit><hex digit><cr><hex digit><hex digit><cr>
```

Write

```
Command : W<hex digit><hex digit><hex digit><hex digit><cr>

Response: W<hex digit><hex digit><hex digit><hex digit><cr>
```

Illegal

```
Response: ?
```

A3 Schematic