Coryell & Wiprud

EV-4014

Quad Receiver Board

Data Sheet

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1.0   Summary of Features

The Coryell & Wiprud EV–4014 is designed to accelerate the evaluation of Graychip's GC4014 Quad Receiver Chip. The GC4014 can be exercised using a simple test setup consisting of the EV–4014, a spectrum analyzer or oscilloscope, and the power supply provided with the board. One of 8 sets of GC4014 register configurations and a variety of several signal sources are selected by dip-switches.

Further testing may be accomplished using the high speed RS–232 port to program the GC4014 and a variety of analog and digital input and output ports. The EV–4014 can be driven digitally by up to four 14 bit, 62.5 MSPS digital input ports, 2 analog inputs driving 12 bit, 41 MSPS, analog to digital converters, or a digital CW or pseudonoise generator. Output signals are monitored using four, 16 bit, 600 KSPS, digital to analog converters, four DSP serial outputs, a 'C40 Comm Port, or a SHARC Link Port. Clocks are derived from one of the digital inputs, an external source, or from an on-board 50 MHz source.

One or more EV–4114 Quad Transmitter Chip Evaluation Boards may be used as digital signal sources for the EV–4014. The EV–4014 and the EV–4114 are a complementary pair of products designed to make your product development faster and easier.

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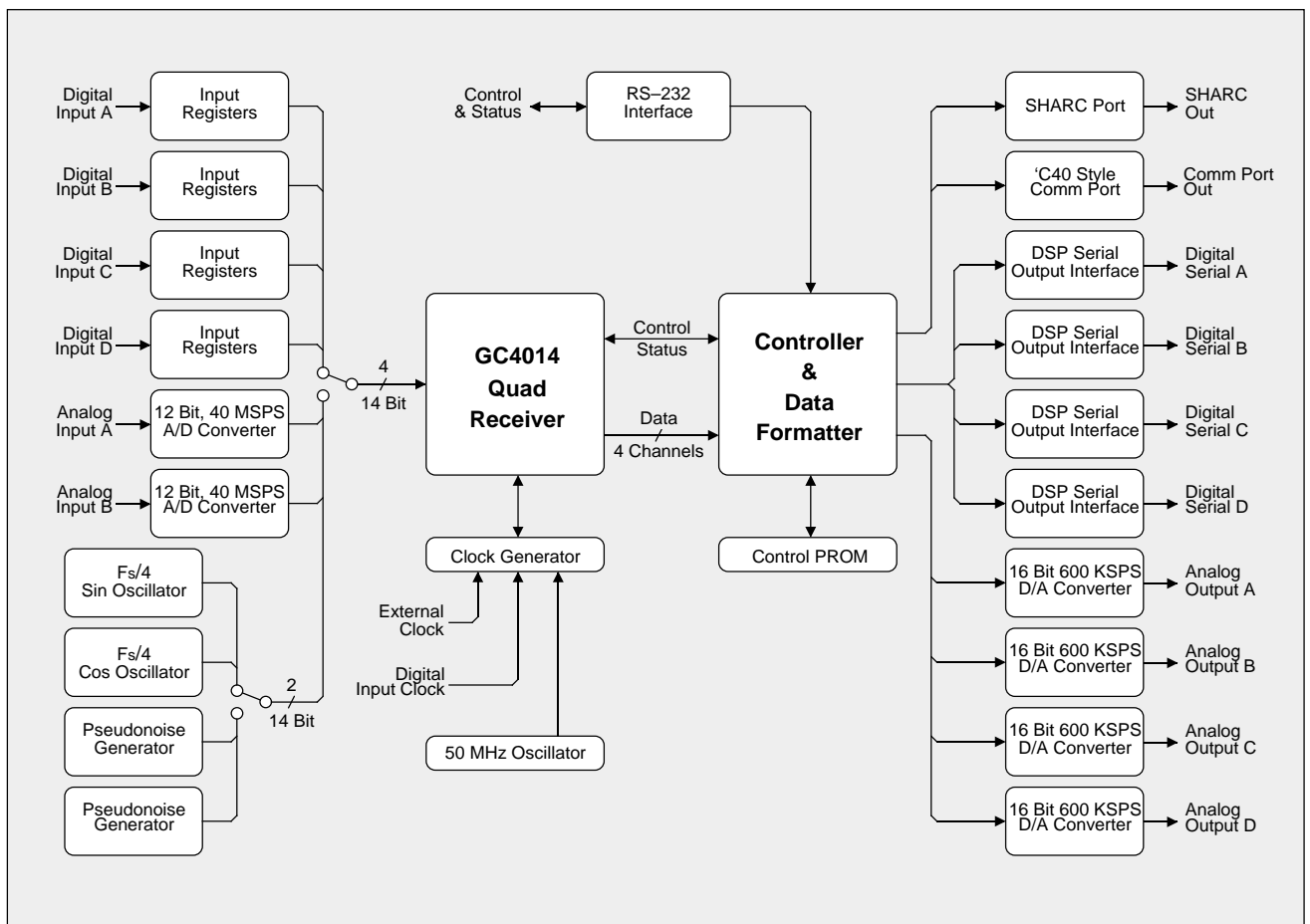
1.1   Summary of Operation

The EV-4014 is designed for stand-alone operation or under manual or computer control. By changing dip switch settings, up to 32 different configurations can be loaded with the push of a button. Additional variations on these 32 basic configurations are possible by selecting various input sources and modulations.

Additionally, there is complete flexibility in configuring the Graychip GC4014 after the EV-4014 has been configured. An external computer can read or write any register within the GC4014 via the RS-232 connector.

1.2   Static Sensitivity Warning

The EV-4014 contains static sensitive circuitry. Do not remove the EV-4014 from its protective shipping wrapper unless in a static-controlled area. Proper static control procedures must be followed to prevent damage to the board, especially during connection of external cabling.

2.0   Preparing the board for operation

As shipped, the EV-4014 board is almost ready to go. To use the board, connect a 5 volt power supply to the connector labeled JPOWER, connect analog inputs to JAD1 and JAD2 (as desired), and monitor the output via the JDA1 through JDA4 connectors.

There are a number of user-configurable settings on the EV-4014, some of which are interlinked. Please take a few moments to familiarize yourself with the switch and jumper settings which follow.

2.1   Switch & Jumper Settings

The following section describes the function of each switch on the board. There is a single pushbutton switch (labeled SLoad), and there are two banks of 8-bit dip switches (labeled S1 and S2 on the board), totaling 16 configuration switches. Each dip switch has been assigned a number in the tables below. For example, S1-3 is the third switch on S1 (where the first switch on S1 is the switch closest to the silk screen label "S1"). The default switch settings have been highlighted in bold in the tables below. In addition to the switches, there are two 2x3 pin jumper blocks used for clock configuration.

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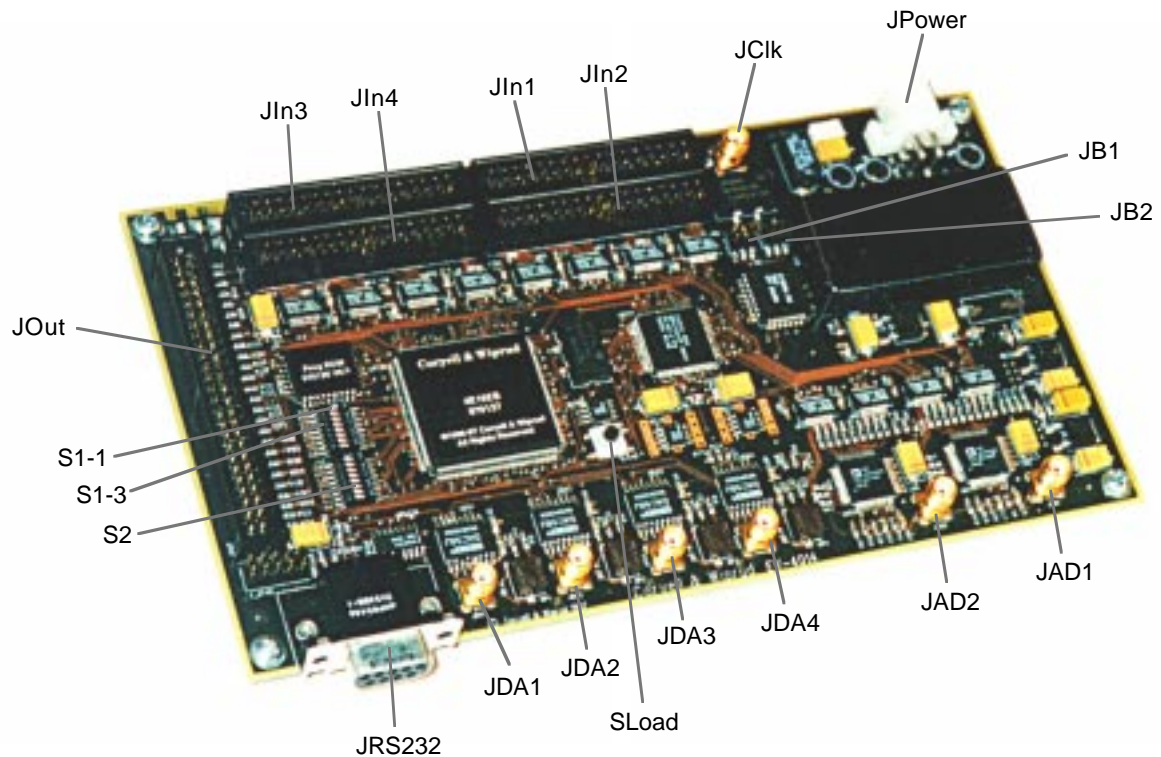
2.2   Load Switch

This pushbutton switch (JLoad) causes the board to be reset. Upon reset, the board will configure the GC4014 based upon the dip switch settings (S1-8..S1-4). Following configuration, the board will be active and will respond to RS-232 commands over JRS2332.

2.3   Configurations Switches

There are 2 sets of 8 configurations switches labeled S1-1 through S1-8 and S2-1 through S2-8 on the board. This section describes the operation of each of these switches. The switches are abbreviated SN-x, where SN is either S1 or S2 and x is switch number on S1 or S2. For example, S1-3 is the third switch (from the silk screened "S1" on S1. A range of switches is abbreviated SN-x..y, where x is the highest numbered switch and y is the lowest numbered switch.

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2.3.1 RS-232 Interface (S1-2..1)

Switch	Setting	Meaning
S1-2..1	Off,Off	9600 Baud RS-232 interface
S1-2..1	**Off,On**	19200 Baud RS-232 interface
S1-2..1	On, Off	57600 Baud RS-232 interface
S1-2..1	On, On	115200 Baud RS-232 interface

The RS-232 interface conforms with the full +/- 12V signaling levels required by the specification. However, the handshake lines (RTS, CTS, DTR, etc.) are not used. The board drives transmitted serial data on to pin 2 of JRS232 (a DB9 female type connector) and expects to receive incoming serial data on pin 3. These signals are transmitted and received relative to the board ground on pin 5. The format of the serial word for both transmission and reception is 1 start bit, 8 data bits, 1 stop bit, and no parity.

There are two commands understood by the RS-232 interface command interpreter—a read and a write. These commands are designed to control the GC4014 with a minimum of overhead, yet allow manual operator control.

The read command is "Raa<CR>" where R is the literal ASCII character 82, aa is an ASCII-HEX address ranging from 00 to 1F, and <CR> represents a carriage return (ASCII character 13). The response to a read command is "Raa<CR>dd<CR>" where dd is an ASCII-HEX representation of the data found at the given address.

The write command is "Waadd<CR>" where W is the literal ASCII value 87 hex, aa is an ASCII-HEX value ranging from 00 to 1F, and <CR> represents a carriage return (ASCII value 13 hex). The response to a write command is identical, namely "Waadd<CR>".

If an illegal character is detected during command entry, the command is aborted and the character "?" (ASCII value 63 hex) is returned.

2.3.2 Reserved (SW3)

Switch	Setting	Meaning
SW3	**Off**	reserved

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2.3.3 Boot Configuration (SW8..4)

The EV-4014 loads one of 32 register configurations into the GC4014 chip at power up or whenever the LOAD (SLoad) button is pressed. The LOAD LED will be illuminated whenever GC4014 registers are being set. These register configurations may serve as reference configurations for development of new configurations. To load a particular configuration, set the configuration number using Switches S1-4 through S1-8, and press the LOAD button.

In order to make developing custom register settings easier, register settings are echoed to the RS-232 port during loading so they may be captured by a terminal emulation program. The user may then modify the settings as desired and download them back to the the EV-4014

Switch	Setting	Meaning
S1-8..4	Decimal	Boot action setting--see text below. (one of 32)
"00000"	0	Base configuration (see section 2.3.3.1)
"00001"	1	Same as 0 but complex output
"00010"	2	Same as 0 but Link Port
"00011"	3	Same as 1 but Link Port
"00100"	4	Same as 0 but Mux Mode 1
"00101"	5	Same as 1 but Mux Mode 1
"00110"	6	Same as 0 but Mux Mode 2
"00111"	7	Same as 0 but Mux Mode 2
"01000"	8	Not Used
"01001"	9	Not Used
"01010"	10	Not Used
"01011"	11	Not Used
"01100"	12	Not Used
"01101"	13	Not Used
"01110"	14	Not Used
"01111"	15	Not Used
"10000"	16	Not Used
"10001"	17	Not Used
"10010"	18	Not Used
"10011"	19	Not Used
"10100"	20	Not Used
"10101"	21	Not Used
"10110"	22	Not Used
"10111"	23	Not Used
"11000"	24	Not Used
"11001"	25	Not Used
"11010"	26	Not Used
"11011"	27	Not Used
"11100"	28	Not Used
"11101"	29	Not Used
"11110"	30	Not Used
"11111"	31	Diagnostic Output (See section 2.3.3.2)

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The configurations described by the above table are useful for stand-alone demonstrations of the GC4014 capabilities. When other configurations are required, they can be invoked via the RS-232 interface.

2.3.3.1 Boot Configuration 0

Boot Configuration 0, the "base configuration", (the dipswitches in their default positions) is decimation of 5000, real output, and real input. Channel A selects A/D 1 or JIn1 for input and is tuned to 1 MHz (for a 50 MHz input sample rate). Channel B selects A/D 2 or JIn2 for input and is tuned to 10 MHz (50 MHz input sample rate). Channel C selects the in–phase part of a FS/4 sinewave, pseudonoise, or JIn3 for input and tuned to Fs/4 plus ~0.1 Hz. Finally, Channel D selects the quadrature part of an Fs/4 sinewave, pseudonoise, or JIn4 for input and is tuned to Fs/4 plus ~0.1 Hz. Since the inputs are treated as real the C and D channel output signals will be 90° out of phase if the their input source is the Fs/4 sinewave. Selection of A/D or pseudonoise versus JInX is discussed in the next few sections. The register settings for Boot Configuration 0 are given in the table below.

Register	Setting	Meaning
0	6A	Deassert All Syncs
1	81	Enable clock doubler, Real
2	E1	LSB of DEC
3	4	MSB of DEC, DEC=0x4E1=1249, N=1250, 4N=5000
4	21	BIG_SCALE=2, SCALE=1
5	0	MSB of gains = 0, gain = 115
6	B5	SFS low, SCK high, Cont, Packed, SCK=1.5625 MHz
7	0	No rounding, No muxing, No summing
8	40	Output Enabled
9	AA	Flush all channels with OS
0A	FF	CNT LSBs
0B	FF	CNT MSBs, COUNT=0xFFFF => Period = 128 * 0x10000
0C	3	Diag source is DC level 0x4000 (when diag bit on)
0D	4	Page = 4 (Channel A)
10	51	LSB (Byte 0) of Frequency
11	B8	(Byte 1) of Frequency
12	1E	(Byte 2) of Frequency
13	5	MSB (Byte 3) of Freq, 0x051EB851 => 999,999.9895 Hz
14	0	LSB (Byte 0) of Phase
15	0	MSB (Byte 0) of Phase, Phase = 0
16	73	Gain LSB = 115 decimal
17	10	Coarse=1, Input is port A
18	AF	Dither OS, NCO OS, Phase always, Freq always
0D	5	Page = 5 (Channel B)
10	33	LSB (Byte 0) of Frequency
11	33	(Byte 1) of Frequency

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12	33	(Byte 2) of Frequency
13	33	MSB freq, Freq = 0x33333333 => 10 MHz
14	0	LSB (Byte 0) of Phase
15	0	MSB (Byte 0) of Phase, Phase = 0
16	73	Gain LSB = 115 decimal
17	11	Input port is B
18	AF	Dither OS, NCO OS, Phase always, Freq always
0D	6	Page = 6 (Channel C)
10	9	LSB (Byte 0) of Frequency
11	0	(Byte 1) of Frequency
12	0	(Byte 2) of Frequency
13	40	MSB (Byte 3) of Freq, 0x40000009 => 12,500,000.11 Hz
14	0	LSB (Byte 0) of Phase
15	0	MSB (Byte 0) of Phase, Phase = 0
16	73	Gain LSB = 115 decimal
17	12	Input port is C
18	AF	Dither OS, NCO OS, Phase always, Freq always
0D	7	Page = 7 (Channel D)
10	9	LSB (Byte 0) of Frequency
11	0	(Byte 1) of Frequency
12	0	(Byte 2) of Frequency
13	40	MSB (Byte 3) of Freq, 0x40000009 => 12,500,000.11 Hz
14	0	LSB (Byte 0) of Phase
15	0	MSB (Byte 0) of Phase, Phase = 0
16	73	Gain LSB = 115 decimal
17	13	Input port is D
18	AF	Dither OS, NCO OS, Phase always, Freq always
0D	4	Page = 4 (Channel A)
0	EA	Turn on Oneshot
0	6A	Use Oneshot; Output, Counter, & Dec sync are Oneshot

2.3.3.2 Boot Configuration 31 (Diagnostic Pattern)

Boot Configuration 31 causes the GC4014 to generate a repeating pattern that can be used to verify serial or Comm port interfaces to DSP chips. This configuration produces 4 channels of Fs/4 outputs, each one at a unique phase. The output from the GC4014 repeats every 2 complex output samples:

```
Output Sample Period 0:

Channel A:  0xEE40 + 0x0000 j
Channel B:  0x0F60 + 0xF720 j
Channel C:  0xF420 + 0xF2D0 j
Channel D:  0xF590 + 0xF1A0 j
```

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```
Output Sample Period 1:

Channel A:   0x11C0 + 0x0000 j
Channel B:   0xF0A0 + 0x08E0 j
Channel C:   0x0BE0 + 0x0D30 j
Channel D:   0x0A70 + 0x0E60 j
```

These data are also seen as the serial data output on JOut. The corresponding Comm port outputs are (in actual time order):

```
Output Sample Period 0:

0x00, 0x00, 0xE0, 0x08, 0x30, 0x0D, 0x60, 0x0E
0x40, 0xEE, 0x60, 0x0F, 0x20, 0xF4, 0x90, 0xF5

Output Sample Period 1:

0x00, 0x00, 0x20, 0xF7, 0xD0, 0xF2, 0xA0, 0xF1
0xC0, 0x11, 0xA0, 0xF0, 0xE0, 0x0B, 0x70, 0x0A
```

Logically, the Comm port outputs are half of an output sample late, so for each output sample period (OSP), the Comm port will output the imaginary part of the previous sample along with the real part of the current sample. This half of an output sample period delay is due to the need to evenly space these same output data for the DACs. The data output by the Comm port is as follows:

```
Output Sample Period 0:

OSP -1 Imaginary part in A,B,C,D order:    0x0000, 0x08E0, 0x0D30, 0x0E60
OSP 0  Real part in A,B,C,D order:         0xEE40, 0x0F60, 0xF420, 0xF590

Output Sample Period 1:

OSP 0  Imaginary part in A,B,C,D order:    0x0000, 0xF720, 0xF2D0, 0xF1A0
OSP 1  Real part in A,B,C,D order:         0x11C0, 0xF0A0, 0x0BE0, 0x0A70
```

Timing-wise, the Comm port data appears for 8 SCK clocks just after RDY, then there is an 8 SCK pause, followed by 8 SCK clocks of more Comm data. The GC4014's SCK phase selection determines where /CSTRB will fall relative to the CD7..0 data. SCK(0) causes /CSTRB to fall in the middle of the bit period, while SCK(1) causes /CSTRB to fall at the beginning of the bit period.

2.3.4 Channel A Input Selection (S2-1)

Switch	Setting	Meaning
S2-1	**Off**	Channel A input data is analog (from A/D 1)
	On	Channel A input data is digital (from JIn1)

Channel A of the GC4014 gets its input data from the first A/D converter which is connected to JAD1 when the switch S2-1 is off. Channel A gets its digital data directly from JIn1 when this switch is on.

2.3.5 Channel B Input Selection (S2-2)

Switch	Setting	Meaning
S2-2	**Off**	Channel B input data is analog (from A/D 2)
	On	Channel B input data is digital (from JIn2)

Channel B of the GC4014 gets its input data from the second A/D converter which is connected to JAD2 when the switch S2-2 is off. Channel A gets its digital data directly from JIn2 when this switch is on.

2.3.6 Channel C Input Selection (S2-3)

Switch	Setting	Meaning
S2-3	**Off**	Channel C input data is sinewave or pseudonoise
	On	Channel C input data is digital (from JIn3)

Channel C of the GC4014 gets its input data from either an internally generated sinewave or pseudonoise generator (depending on the position of S2–5) when switch S2-3 is off. Channel A gets its digital data directly from JIn1 when this switch is on.

2.3.7 Channel D Input Selection (S2-4)

Switch	Setting	Meaning
S2-4	**Off**	Channel D input data is sinewave or pseudonoise
	On	Channel D input data is digital (from JIn3)

Channel D of the GC4014 gets its input data from either an internally generated sinewave or pseudonoise generator (depending on the position of S2–5) when switch S2-4 is off. Channel A gets its digital data directly from JIn1 when this switch is on.

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2.3.8 Sinewave or Pseudonoise Generator Select (S2-5)

Switch	Setting	Meaning
S2-5	**Off**	Generate Sinewave (I on Chan C and Q on Chan D)
	On	Generate Pseudonoise (I on Chan C and Q on Chan D)

When this switch is off, a complex sinewave at Fs/4 is generated. Complex pseudonoise is generated when S2-5 is on. This switch only has an effect on channel C if switch S2-3 is off, and for channel D if switch S2-4 is off. Complex data is only processed if the GC4014 is configured for complex data input (please see the GC4014 datasheet), otherwise the input data is interpreted by the GC4014 as a real sinewave input as Fs/4 or real pseudonoise.

2.3.9 Reserved (S2-6)

Switch	Setting	Meaning
S2-6	**Off**	Reserved

2.3.10 PLL Frequency Range (S2-7)

Switch	Setting	Meaning
S2-7	Off	GC4014 Operates in 25-50 MHz range
	On	GC4014 Operates in 40-62.5 MHz range

Set this switch to match the frequency of operation for the board. Normal operation from the on-board crystal oscillator will require this switch to be on. This switch may have to be changed if a slower external clock is used (see JB1 jumper settings).

2.3.11 PLL Disable (S2-8)

Switch	Setting	Meaning
S2-8	**Off**	PLL enabled for normal operation (25 to 62.5 MHz)
	On	PLL disabled (<25 MHz)

The on-board PLL circuit locks to a clock reference (as selected by the JB1 jumper) and provides zero-skew clocks to all circuits on the board. Disabling the PLL makes it operate like a buffer, introducing a delay between the reference clock and those on the board. This switch S2-8 should be turned on if the external clock frequency is less than 25 MHz, but needs to be off otherwise.

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2.4   Clock Source Selection (JB1)

The board obtains a clock from an on-board 50 MHz crystal oscillator, a digital input (JIn1), or from an external source (JCLK). The selection is done via a jumper block (JB1) as follows:

JB1   **JB1**   **JB1**

Clock From JIn1   Clock From   Clock From JCLK
                        Internal Oscillator
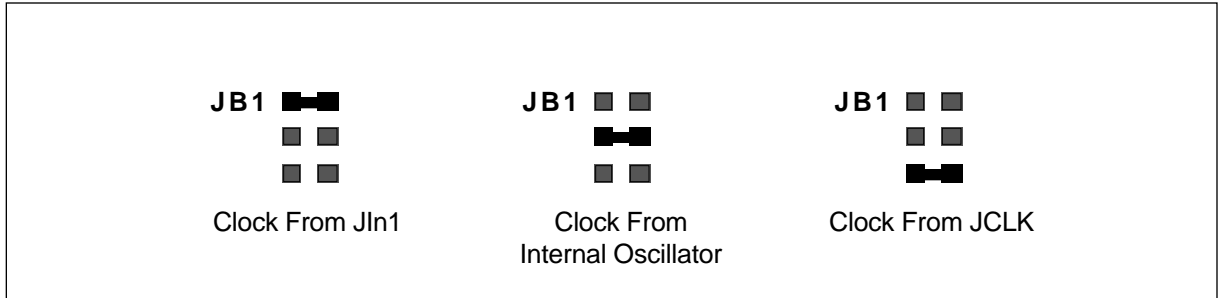
Use the silk screened label "JB1" as a reference for determining the correct jumper position.

2.5   Reserved (JB2)

The jumper block JB2 is reserved and should have no jumpers installed. The board will not operate correctly if a jumper is installed on JB2.

JB2

Reserved
(No jumpers installed)
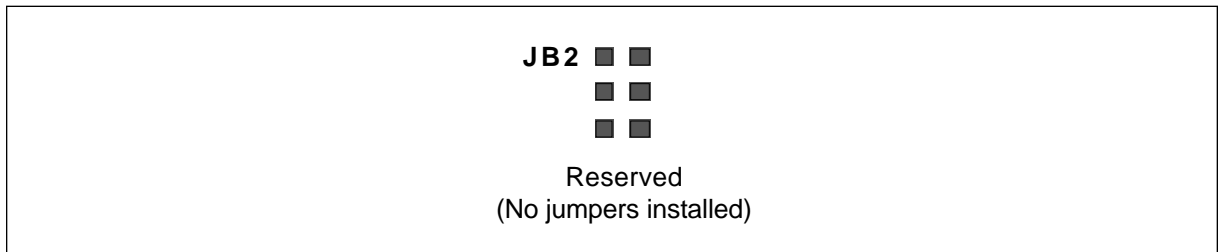
3.0   Input Requirements

3.1   Analog Inputs (JAD1-2)

      Input range: 1V (peak to peak)

      Input impedance: 50 Ω

      Connector type: SMA

3.2   Digital Inputs (JIn1-4)

Input type: TTL, Single-ended, 14 bit 2's complement

Timing requirements: 5 ns setup, 3 ns hold, data is registered on the rising edge of the clock, the clock source for the input registers for each channel is provided by that channel's clock. The clock used by the rest of the board is selected by JB1.

Connector type: 34-pin IDC

Pinout: see below.

Pin	Type	Name	Function
1	N/C		
3	I	D13	Data MSB
5	I	D12	Data
7	I	D11	Data
9	I	D10	Data
11	I	D9	Data
13	I	D8	Data
15	I	D7	Data
17	I	D6	Data
19	I	D5	Data
21	I	D4	Data
23	I	D3	Data
25	I	D2	Data
27	I	D1	Data
29	I	D0	Data LSB
31	I	Sync/NC	External Sync on JIn1, No Connection on JIn2-4
33	I	Clock	Data is registered on the rising edge of this clock
Even	Pwr	Ground	All even pins are ground

3.3   External Clock (JCLK)

Input type: TTL, 50Ω

Connector type: SMA

3.4　External Commands RS-232 (JRS232)

Input/Output type:　　　RS-232, +/- 12V

Connector type:　　　　DB9 Female

Pinout:

Pin	Type	Name	Function
1	N/C		
2	O	TxD	Transmitted data
3	I	RxD	Received data
4	N/C		
5	Pwr	Ground	Ground reference
6	N/C		
7	N/C		
8	N/C		
9	N/C		

3.5　Power Input (JPOWER)

Input requirement:　　　+5 Volts +/- 5% only, < 4 amperes.

Connector type:　　　　4 Wire Power Socket (use the power supply provided with the board).

Pinout:

Pin	Type	Name	Function
1	Pwr	+5V	Board main power source
2	N/C		
3	Pwr	Ground	Board main power return
4	N/C		

4.0　Outputs

4.1　Comm Port (JOut)

Output type:　　　　　TTL, 49Ω series termination

Timing requirements:　As specified by Texas Instruments for the

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TMS320C4x processor series.

Connector type: 40-pin IDC

Pinout: Please see the figure below.

4.2   Link Port (JOut)

Output type: TTL, 49Ω series termination

Timing requirements: As specified by the GC4014 Datasheet.

Connector type: 40-pin IDC

Pinout: Please see the figure below.

4.3   GC4014 Outputs (JOut)

Type: TTL, 49Ω series termination

Timing Requirements: As specified by the GC4014 Datasheet (with a 49Ω series resistor).

Connector type: 40-pin IDC

Pinout: Please see the figure below.

4.3   Serial Outputs (JOut)

Type: TTL, 49Ω series termination

Timing Requirements: +/-3 ns skew between SerClk, /LE, and Serial Data

Connector type: 40-pin IDC

Pinout: Please see the figure below.

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Pin	Type	Name	Function
1	I/O	RDY/ACK	RDY/ACK pin on GC4014
3	O	SCK	SCK pin on GC4014
5	O	SFS	SFS pin on GC4014
7	O	L3/A	L3/A pin on GC4014
9	O	L2/B	L2/B pin on GC4014
11	O	L1/C	L1/C pin on GC4014
13	O	L0/D	L0/D pin on GC4014
15	O	SerClk	Serial Port Clock
17	O	/LE	Frame Sync (falling edge marks beginning of MSB)
19	O	SerA	Serial data for channel 1
21	O	SerB	Serial data for channel 2
23	O	SerC	Serial data for channel 3
25	O	SerD	Serial data for channel 4
27	O	/CREQ	Comm Port Mastership Desired
29	I	/CACK	Comm Port Granted
31	O	/CSTRB	Comm Data Valid
33	I	/CRDY	Comm Data Accepted
35	O	D7	Comm Port Data Bit 7 (MSB)
37	O	D6	Comm Port Data Bit 6
39	O	D5	Comm Port Data Bit 5
41	O	D4	Comm Port Data Bit 4
43	O	D3	Comm Port Data Bit 3
45	O	D2	Comm Port Data Bit 2
47	O	D1	Comm Port Data Bit 1
49	O	D0	Comm Port Data Bit 0 (LSB)
Even	Pwr	Ground	All even pins are ground

4.2   Analog Outputs (JDA1-4)

Output voltage range: ± 3 V (peak) into 1 MΩ

Connector type: SMA

4.3   Power LED (DSPwr)

Illuminated while +5V supply is present.

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4.4   Loading LED (DSLoad)

Illuminated while Graychip GC4014 is being configured from ROM. After this light
goes out, RS-232 commands will be accepted. While any command from the RS-232
interface is in progress, this LED will be illuminated.

4.5   Reserved LED (DS1)

DS1 is reserved and its state has no meaning.

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Appendices

A1   ROM Formats

UROM - ASCII commands identical to the RS-232 format. 32 possible different programs, each starting at a unique address. Each program must be zero terminated. Coryell & Wiprud can burn your custom GC4014 register configurations into the ROM.

A2   RS-232 Command Format

RS-232 command formats There are 6 bits of address used by the GC4014, so valid addresses are from 0x00 to 0x3F.

Read

```
Command : R<hex digit><hex digit><cr>

Response: R<hex digit><hex digit><cr><hex digit><hex digit><cr>
```

Write

```
Command : W<hex digit><hex digit><hex digit><hex digit><cr>

Response: W<hex digit><hex digit><hex digit><hex digit><cr>
```

Illegal

```
Response: ?
```